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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,466	02/28/2002	Hiroyuki Matsumoto	ASAM.0041	4986

7590 06/21/2006

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EXAMINER	
NGUYEN, LUONG TRUNG	
ART UNIT	**PAPER NUMBER**
2622	

DATE MAILED: 06/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,466	MATSUMOTO ET AL.	
	Examiner	Art Unit	
	LUONG T. NGUYEN	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6 and 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6, 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Upon thorough the examination of the claims 6 and 12 and Kasahara et al. reference, and the final office action mailed on 3/07/06, the Examiner finds that Kasahara et al. reference still can read on claims 6 and 12 with different interpretation in reading Kasahara et al. reference. Therefore, the final office action mailed on 3/07/06 has been withdrawn. However, upon further consideration a new non-final office action sets forth below.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 6 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Kasahara et al. (U. S. Patent No. 6,710,818).

Regarding claim 6, Kasahara et al. discloses an imaging system including a solid-state CMOS imaging device and a signal processing semiconductor integrated circuit for processing read-out signals of pixels from said solid-state CMOS imaging device, comprising:

first level detection means which detects brightness on a first area (a horizontal line) set up on an imaging area of said solid-state CMOS imaging device (the flicker judging circuit 5

judges whether illumination flicker exist in the video signal by frequency analyzing the dividing results of horizontal lines, Column 8, Lines 5-32, Column 2, Lines 30-55).

second level detection means which detects brightness on a second area (a plurality of horizontal lines) larger than first area (the flicker judging circuit 5 judges whether illumination flicker exist in the video signal by frequency analyzing the dividing results of horizontal lines, Column 8, Lines 5-32, Column 2, Lines 30-55).

judgment means which judges turning-on-and-off of a light source illuminating (judging flicker) an object to be imaged on the basis of detection levels of said first and second level detection means (the flicker judging circuit 5 judges whether illumination flicker exist in the video signal by frequency analyzing the dividing results of horizontal lines, Column 8, Lines 5-32, Column 2, Lines 30-55).

a control unit for setting up an electric charge storage time for each pixel of said solid-state CMOS imaging device by means of processing in accordance with a program (the flicker compensation signal generation apparatus 90 determines shutter speed according with the flicker frequency is 50 Hz or 60 Hz according to loops including the steps s3 to s10 in the flow chart (a program) of figure 17, figure 16, column 15, line 51 – column 16, line 45. Note that in operating a CMOS image sensor, the shutter speed determines the charge storage time).

wherein said judgment of the turning on-and off of said light source illuminating in accordance with the object on the basis of the detection levels of said first and second detection means is performed by processing in accordance with the program in said control unit (the flicker detection circuit detects illumination flicker based on the level of signal according to the flow chart (a program) of figure 17, figure 16, column 15, line 51 – column 16, line 45).

Regarding claim 12, Kasahara et al. discloses an imaging system including a solid-state CMOS imaging device and a signal processing semiconductor integrated circuit for processing read-out signals of pixels from said solid-state CMOS imaging device, comprising:

first level detection means which detects brightness on a first area (a horizontal line) set up on an imaging area of said solid-state CMOS imaging device, the first area which is predetermined area in a frame (the flicker judging circuit 5 judges whether illumination flicker exist in the video signal by frequency analyzing the dividing results of horizontal lines, Column 8, Lines 5-32, Column 2, Lines 30-55).

second level detection means which detects brightness on a second area (a plurality of horizontal lines) which is set up on an imaging area of said solid-state CMOS imaging device, and is larger than first area, the second area which is a predetermined area in the frame (the flicker judging circuit 5 judges whether illumination flicker exist in the video signal by frequency analyzing the dividing results of horizontal lines, Column 8, Lines 5-32, Column 2, Lines 30-55).

judgment means which judges turning-on-and-off of a light source illuminating (judging flicker) in accordance with an object to be imaged on the basis of detection levels of said first and second level detection means (the flicker judging circuit 5 judges whether illumination flicker exist in the video signal by frequency analyzing the dividing results of horizontal lines, Column 8, Lines 5-32, Column 2, Lines 30-55).

a control unit for setting up an electric charge storage time for each pixel of said solid-state CMOS imaging device by means of processing in accordance with a program (the flicker

compensation signal generation apparatus 90 determines shutter speed according with the flicker frequency is 50 Hz or 60 Hz according to loops including the steps s3 to s10 in the flow chart (a program) of figure 17, figure 16, column 15, line 51 – column 16, line 45. Note that in operating a CMOS image sensor, the shutter speed determines the charge storage time).

wherein said judgment of the turning on-and off of said light source illuminating in accordance with the object on the basis of the detection levels of said first and second detection means is performed by processing in accordance with the program in said control unit (the flicker detection circuit detects illumination flicker based on the level of signal according to the flow chart (a program) of figure 17, figure 16, column 15, line 51 – column 16, line 45).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LUONG T. NGUYEN whose telephone number is (571) 272-7315. The examiner can normally be reached on 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID L. OMETZ can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LN
06/15/06

LUONG T. NGUYEN
PATENT EXAMINER